STATIC PASS TRANSISTOR LOGIC WITH TRANSISTORS WITH MULTIPLE VERTICAL GATES

Abstract of the Disclosure

Static pass transistor logic having transistors with multiple vertical gates are described. Multiple vertical gates are edge defined with only a single transistor being required for multiple logic inputs. Thus a minimal surface area is required for each logic input. The static pass transistor includes a transistor which has a horizontal depletion mode channel region between a single source and drain region. A number of vertical gates are located above different portions of the depletion mode channel region. A vertical gate is located above a first portion of the depletion mode channel region and is separated therefrom by a first insulator material. A vertical gate is located above a second portion of the channel region and is separated therefrom by a second insulator material. There is no source nor drain region associated with each input and the gates have sub-lithographic horizontal dimensions by virtue of being edge defined vertical gates.

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